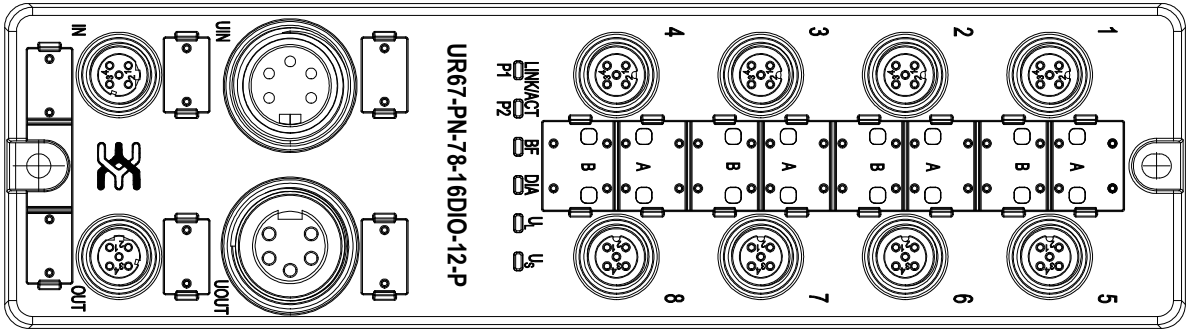




| 接线示意图          |  | 接口定义说明                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PNP输入<br>(2线制) |  | <div>M12x8 I/O</div> <div><div><div>1</div><div>2</div><div>3</div><div>4</div><div>5</div></div><div>Pin1 +24V<br/>Pin2 DI<sub>I</sub>/DO<sub>I</sub><br/>Pin3 GND 0V<br/>Pin4 DI<sub>A</sub>/DO<sub>A</sub><br/>Pin5 FE</div></div>                                                                                                                                                                      |
| PNP输入<br>(3线制) |  |                                                                                                                                                                                                                                                                                                                                                                                                            |
| PNP输出          |  |                                                                                                                                                                                                                                                                                                                                                                                                            |
| 供电             |  | <div>7/8" POWER</div> <div><div><div>1</div><div>2</div><div>3</div><div>4</div><div>5</div></div><div>Pin1 GND U<sub>L</sub><br/>Pin2 GND U<sub>S</sub><br/>Pin3 FE(PE)<br/>Pin4 +24V U<sub>L</sub><br/>Pin5 +24V U<sub>L</sub></div></div> <div>M12x2 NET</div> <div><div><div>1</div><div>2</div><div>3</div><div>4</div></div><div>Pin1 TD+<br/>Pin2 RD+<br/>Pin3 TD-<br/>Pin4 RD-<br/>BUS</div></div> |

The reproduction, distribution and utilization of this document as well as the communication of its contents to others without explicit authorization is prohibited.  
Offenders will be held liable for the payment of damages. Weidmueller exclusively reserves the right to file for patents, utility models or designs.

© Weidmueller Interface GmbH & Co. KG

General Tolerances:

Changes: PLM

Mat. No. (SAP) 3076250000

PLM

Drawn PLM

Responsible PLM

Approved PLM

Tolerances ISO 8015

**Weidmüller**

PLM  
Drawing no.  
Scale: ..  
Sheet 1 / 1

UR67-PN-78-16DIO-12-P